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EP 0 224 013 A2

⑲ Method for producing coplanar multi-level metal/insulator films on a substrate.

⑳ The method comprises the following steps:  
providing a substrate (3) having an underlying metal-  
lization (4) therein; placing an insulator (5, 6, 8) on  
said substrate (3); selectively removing first portions  
of said insulator at first locations, said first portions  
partially penetrating through said insulator; selec-  
tively removing second portions of said insulator at

second locations, said second portions penetrating  
fully through the remainder of said insulator; said  
second portions being in alignment with some of  
said first portions; simultaneously depositing metal -  
(9) over said insulator to form said overlying metal-  
lization in said first locations and said stud via  
connections in said second locations, and removing any

of said metal (9) which overlies said insulator at locations other than said first locations. The method is applied for forming simultaneously an overlying metallization pattern and stud via connections to an underlying metallization.

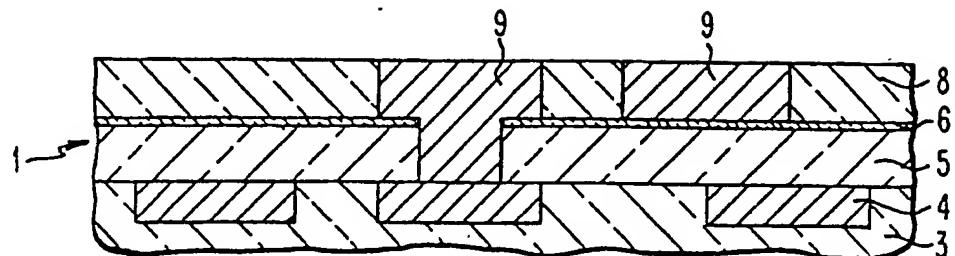


FIG. 6

### Method for Producing Coplanar Multi-Level Metal/Insulator Films on a Substrate

The present invention relates to the manufacture of semiconductor chips in general.

A semiconductor chip consists of an array of devices whose contacts are interconnected by patterns of wiring metal stripes. In VLSI chips, these metal patterns are multi-layered and separated by layers of insulating material. Interconnections between different levels of metal wiring patterns are made by holes (or via holes), which are etched through said layers of insulating material. Typical chip designs consist of one or two wiring levels, with three wiring levels being the current state of the art. Circuit cost and performance requirements continue to place demands on the fabrication processes in such a way that the addition of supplementary wiring levels must remain competitive even though additional processing steps are involved. However, the existing technique of using via-holes has multiple limitations and drawbacks in that, as the number of metallization layers increases, wiring becomes increasingly difficult, as may be clearly understood from Fig. 1.

The semiconductor structure 10 shown in Fig. 1 is a typical example of said current state of the art technology. It is comprised of a silicon substrate 11 of a predetermined conductivity type having a patterned first insulating layer 12 of silicon dioxide ( $\text{SiO}_2$ ) thereon. The first level of metallization is represented by a metal land 13 which makes contact through via hole 14 with a region 15 of the substrate. It makes contact, for example as an ohmic contact, with the emitter region of a bipolar transistor (not represented).

The second level of metallization represented by metal land 16 makes an electrical contact with metal land 13 through via hole 17 of the second insulating layer 18. The structure is passivated with a third insulating layer 19. Although the structure depicted in Fig. 1 is not to scale, it exemplifies the very irregular surface, far from planar, which results from the standard process.

With such a non-planar structure, the known problems are: first a risk of a potential short at location A between the first and second levels of metallization, due to the thinning of the insulating layer therebetween, and second the risk of a potential open circuit at location B, due to the thinning of the metal layer at that location (so called necking effect). Those risks are unacceptable for the high standard of reliability which are required in that industry. Therefore there is a present and serious need to improve the via-hole technique to solve the acute problem of planarizing such irregular surfaces.

Separate processes typically are used for making a given patterned metal level and for making stud via connections from the given level to a latter formed overlying patterned metal level. One example of such processes is described in *Process for Multilayer Metal Technology*, by G. T. Chiu et al., IBM Technical Disclosure Bulletin, Vol. 25, No. 10, March 1983, pg. 5309. According to the described technique, a lower level metal contact or conductive pattern is formed in an insulator layer, stud connectors are fabricated at selected locations of the lower level metal pattern, insulator material is placed about the stud connectors, an overlying insulator layer is deposited and patterned, and an upper level metal or other conductive pattern is placed in the overlying insulator layer. Not only is the cited technique complicated and costly but the planarization of the individual metal and stud levels is difficult to accomplish.

It is the object of the invention to provide a simple reliable method for producing coplanar multi-level metal/insulator films on a substrate by which conductive lines as well as stud via metal contacts are simultaneously formed. This object is achieved by a method as defined in claim 1. The inventive method is especially suitable for application in the manufacturing of high performance VLSI semiconductor chips.

Preferably the method is conducted in the following way:

A first planarized layer of insulation is deposited over a first level of patterned conductive material to which contacts are to be selectively established. The first layer then is covered by an etch stop material. Contact holes are defined in the etch stop material using conventional photolithography at locations where stud connectors are required. The thickness of the first layer of insulation is made equal to the desired stud height. The first layer of insulation is not etched at this time.

Next, a second planarized layer of insulation, having a thickness equal to the thickness of the second level of patterned conductive material of the multi-level structure, is deposited over the etch stop material. The second layer insulation, in turn, is etched by photolithography down to the etch stop material to define desired wiring channels, some of which will be in alignment with the previously formed contact holes in the etch stop material. In those locations where the contact holes are exposed, the etching is continued into the first layer of insulation to uncover the underlying first level of patterned conductive material.

The channels and via holes etched into the second and first layers of insulation, respectively, are overfilled with metallization. The excess metallization, on top of the second layer of insulation but not in the channels or via holes is removed by etching or by chem-mech (chemical-mechanical) polishing. In the case of etching, the same tool used for the deposition of the overfilled metallization can be adapted for in-situ plasma mode etching of the excess metallization. Chem-mech polishing can be achieved following the teachings described in EU Patent Application Serial Number 86 110 461.0 to K.D. Beyer et al with the title "Chem-Mech Polishing Method For Producing Coplanar Metal/Insulator Films On A Substrate", the disclosure of which is incorporated herein by reference.

A method is disclosed in this European application for producing coplanar metal/insulator films on a substrate according to a chem-mech polishing technique. In one example a substrate having a patterned insulating layer of dielectric material thereon is coated with a layer of metal. The substrate is then placed on a parallel polisher, e.g. in the one described in the IBM Technical Disclosure Bulletin, Volume 15, No. 6, November 1972, pp. 1760 -1761, and the metal is removed elsewhere except in the holes of the pattern where it is left intact. This is made possible through the use of an improved selective slurry which removes the metal much faster than the dielectric material. The insulating layer may then be used as an automatic etch stop barrier.

If the material to be polished a metal, like Al or its alloys, a slurry comprising an acetic solution of dispersed silica particles or alumina powder is used. The solution has a pH of less than 3 and the acid used is selected from the group H<sub>2</sub>SO<sub>4</sub>, CH<sub>3</sub>COOH and HNO<sub>3</sub>. In the application also the chem-mech polishing of insulators like quartz is described. If for example quartz to be polished with a large removal rate and a metal, like Al-Co with a small removal rate, an appropriate slurry comprises a basic solution (pH 11 to 11.5) of potassium hydroxide and silica particles.

Chem-mech polishing processes with large removal rates ratios can be found for many combinations of metals and dielectric materials. The advantages of the chem-mech technique are that it is faster than lift-off processes, less extensive and extendable to finer dimensions.

Other advantageous embodiments of the inventive method are disclosed in the subclaims.

Fig. 1 shows a schematic cross-sectional view of a multilayered metal semiconductor structure fabricated according to standard processes and exhibiting a typical non-planar surface.

Figs. 2-6 are a series of simplified cross-sectional views of the formation of coplanar multi-level metal/insulator films on a substrate resulting at successive stages during the course of the method of the present invention.

Fig. 2 shows a structure 1 which typically includes a substrate 2 consisting of a first planarized layer 3 of dielectric material deposited over a first level 4 of patterned conductive material. In a general case, conductors 4 may or may not penetrate fully through insulation 3 which, in turn, is located over an integrated circuit chip. In the former instance conductors 4 would be contact metallurgy to devices (not shown) formed in the chip. In the latter instance (shown) conductors 4 would be a level of metallization insulated from the chip surface. As is well understood, insulation 3 commonly comprises planarized SiO<sub>2</sub> or reflowed phosphosilicate glass whereas conductors 4 typically are copper-doped aluminum or doped polycrystalline silicon. The specific nature of insulation 3 and conductors 4 is not of moment to the present invention.

A first planarized layer of insulation 5, such as sputtered quartz, is deposited over substrate 2 in a thickness equal to the desired height of stud via connections.

A thin layer of etch stop material 6, such as aluminum oxide, is deposited and patterned so as to provide a window 7 at each location where a stud via connection is to be formed between underlying metallization level 4 and an overlying metallization level (not shown in Fig. 2) to be deposited later. In preparation for the overlying metallization level, a second planarized layer of insulation 8, for example sputtered quartz or a composite Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> layer (deposited by CVD), is placed down, as shown in Fig. 3, over the structure shown in Fig. 2. The thickness of layer 8 determines the thickness of an overlying level of metallization to be formed in channels to be etched completely through layer 8.

Channels are defined by standard photolithography in a resist layer (not shown) over layer 8. In places where a stud via connection to underlying metallization 4 is desired, the respective channel opening in layer 8 must be aligned with a hole (such as hole 7) in etch stop layer 6. To facilitate the alignment, the channel width is wider than the hole, as shown in Fig. 4. The etching of the layer 8 terminates at the etch stop layer where no via is needed. In the case where the layer 8 is sputtered quartz and the etch stop layer is Al<sub>2</sub>O<sub>3</sub>, reactive ion etching using CF<sub>4</sub>/O<sub>2</sub> is appropriate.

After the channels are defined, an overlying level of metallization 9, e.g., Al-Cu, Al-Si or Tungsten is deposited over the structure of Fig. 4 as shown in Fig. 5. The thickness of metallization 9 is

at least as great as the height of the stud via connection 10 (equal to the thickness of layers 5 and 6) plus the thickness of the underlying metallization 5. In the event that layer 5 is CVD Tungsten, the same tool used to deposit the Tungsten also can be used to etch it back in situ in a plasma mode so as to coplanarize the surfaces of layers 8 and 9. Alternatively, layer 9 may be planarized by the chem-mech method taught in copending EU Patent Application Serial Number 86 110 461.0. The result is shown in Fig. 6.

A final thin passivation insulator is required on top of the metal pattern 9 if it is the final metal level. If the wiring level of pattern 9 is to be followed by one or more additional wiring levels, then the above described stud via and overlying metallization steps plus the associated insulation layer steps are repeated for each additional wiring level.

Although the preferred method described with the aid of Figs. 2-6 makes use of etch stop layer 6 and insulation layers 5 and 8, the method may be practiced satisfactorily without the extra steps associated therewith. Instead, a single insulation layer having a thickness equal to the sum of layers 5 and 8 can be deposited on substrate 2. Then, the same photolithography can be used (as produced the pattern in insulator 8 of Fig. 4) while stopping the etching of the single insulation layer when the desired depth for conductors 9 of Fig. 6 is reached. The additional etching of the single insulation layer (to open stud via holes where required) can be accomplished by additional photolithography corresponding to that used to open hole 7 of Fig. 2. The same metallization and planarization steps of Figs. 5 and 6 can then be applied.

Although the preferred embodiment also makes use of sputtered quartz or composite  $\text{Si}_3\text{N}_4/\text{SiO}_2$  for insulation layers 5 and 8, other insulation materials, such as spin-on polyimides, also are suitable. Compatible etch stop layer materials include spin-on glass and plasma nitride where polyimide insulation is used.

### Claims

1. A method for producing multi-level coplanar metal/insulator films comprising the steps of: providing a substrate (3) having an underlying metallization (4) therein; placing an insulator on said substrate; selectively removing first portions of said insulator at first locations where an overlying metallization is desired, said first portions partially penetrating through said insulator; selectively removing second portions of said insulator at second locations where stud via connec-

tions are desired, said second portions penetrating fully through the remainder of said insulator; said second portions being in alignment with some of said first portions;

5 simultaneously depositing metal (9) over said insulator to form said overlying metallization in said first locations and said stud via connections in said second locations, and  
removing any of said metal (9) which overlies said insulator at locations other than said first locations.

2. The method defined in claim 1 wherein said removing is accomplished by chemical-mechanical polishing.

3. The method defined in claim 1 or 2 wherein  
15 said insulator comprises:  
a first insulator layer (5);  
an etch stop layer (6), and  
a second insulator layer (8).

4. The method defined in claim 3 wherein said  
20 first portions are removed from second layer (8), and  
said second portions are removed from said etch  
stop layer (6) and said first layer (5),  
said first layer (5) being adjacent said substrate (3).

25 5. The method defined in claim 3 or 4 wherein  
said first and second layers (5, 8) are quartz, and  
said etch stop layer (6) is  $\text{Al}_2\text{O}_3$ .

6. The method defined in any one of claims 3  
to 5 wherein said first layer (5) is selected from the  
30 group comprised of sputtered quartz,  
phosphosilicate glass and polyimide,  
said second layer (8) is selected from the group  
comprised of quartz, polyimide and a composite  
consisting of  $\text{Si}_3\text{N}_4$  and  $\text{SiO}_2$ , and  
35 said metal (9) is selected from the group com-  
prised of Al-Cu, Al-Si and Tungsten.

7. The method defined in any one of claims 1  
to 6 wherein said insulator is planarized.

8. The method defined in one of claims 1 to 7  
40 wherein said steps other than said step of providing  
said substrate are repeated in sequence a  
desired number of times.

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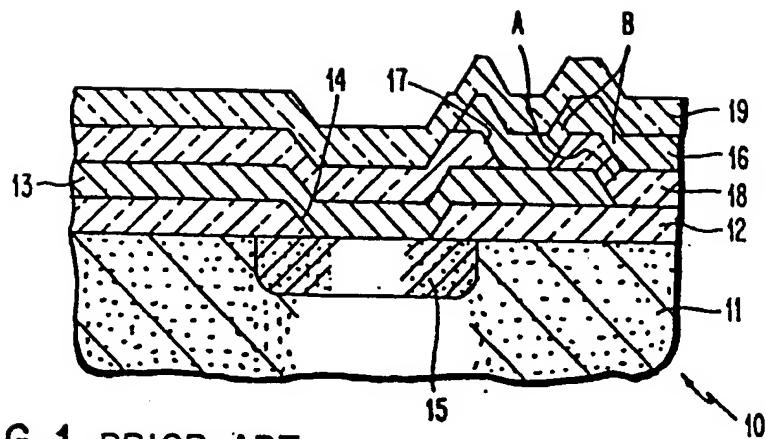
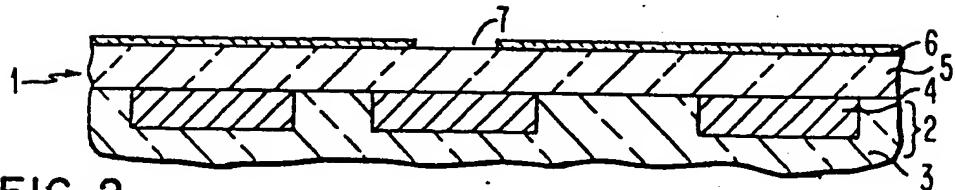
FIG. 1 PRIOR ART

FIG. 2

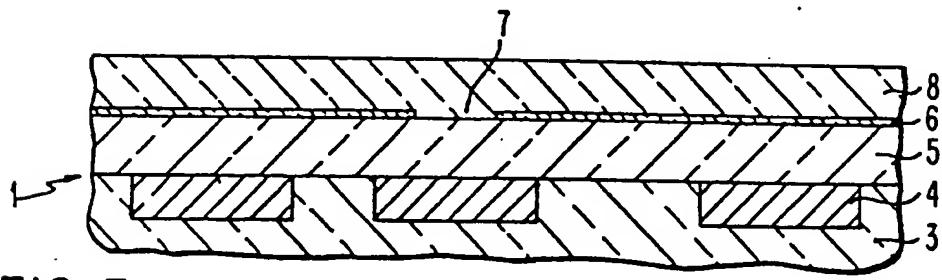


FIG. 3

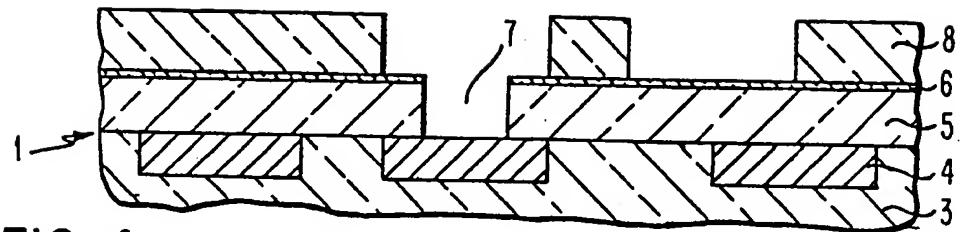


FIG. 4

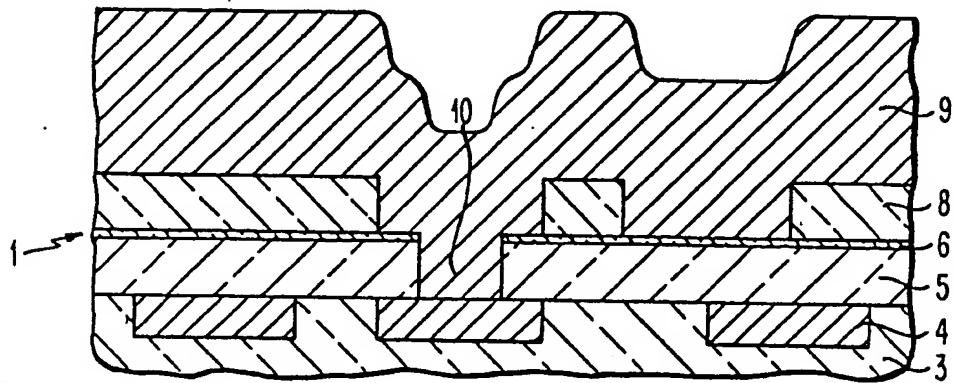


FIG. 5

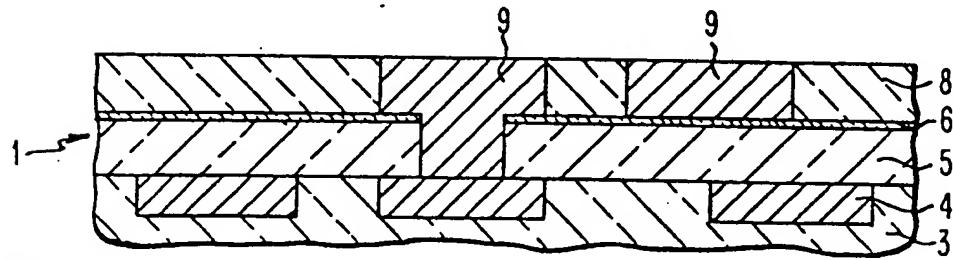


FIG. 6